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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 9

Application Number: 09/589,930
Filing Date: June 07, 2000
Appellant(s): DAY, BRIAN A.

Harold C. Moore
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 16 October 2003.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because "real-time" is only used in the preamble of claim 7 and does not limit the scope of the claims since the preamble does not provide antecedent basis, the language of the body of claims 7-12 set out the complete invention, the preamble merely provides a statement of purpose and the preamble is not necessary in understanding limitations or terms in the claim.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

4,561,095	KHAN	12-1985

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Khan, Aurangzeb K. (US 4561095 A).

35 U.S.C. 102(b) rejection of claim 1.

Khan teaches a test circuit for inclusion on an integrated circuit comprising (col. 3, lines 34-43, Khan): a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence (in Figure 1 of Khan, Khan teaches a device for inserting a parity code into a sequence of data word inputs inputted through terminals D_0, D_1, D_2 and D_3; Figure 1 and col. 6, lines 60-68 in Khan teach that inputs to D_0 and D_1 are used to identify a data unit of a data unit sequence inputted to D_0, D_1, D_2 and D_3 during special test modes such as the special test mode for testing of the error

check logic; in col. 15, lines 58-60 of Khan, Khan explicitly teaches, "means are provided for enabling the deliberate insertion of an erroneous data bit, to provide a real time electronic simulation of a 'soft' error", hence Khan teaches the deliberate insertion of erroneous bits into an identified data unit belonging to a real-time sequence of data units inputted through terminals D_0, D_1, D_2 and D_3 for real-time testing of the error check logic; in col. 18, lines 25-30, Khan teaches that special test modes are accessed by multiplexing inputs to D_0 and D_1, which can be done since special test modes are performed during read access, hence, during special test modes, words inputted to D_0, D_1, D_2 and D_3 are not a next data unit of the data unit sequence stored in memory since they are not written to memory; Figure 1 and col. 6, lines 60-68 in Khan teach that inputs to D_0 and D_1 are used to identify a data unit of a data unit sequence inputted to D_0, D_1, D_2 and D_3 during special test mode wherein the identified data word is not a next data unit of the data unit sequence stored in memory since, during special test mode, the identified data unit is not written to memory, hence the Test Function Generator is a data unit identifier since it identifies a data unit according to multiplexed data inputs D_0 and D_1 and the special test to be applied to the Integrated circuit using the Data Unit inputted through D_0, D_1, D_2 and D_3; Note: the IEEE Authoritative Dictionary of IEEE Standards Terms defines a sequence as a set of items that have been put in a linear arrangement in accordance with the natural numbers, i.e., an ordered set; Note also; that words in memory are an ordered set arranged according to their addresses in memory, hence the set of input of words is inherently a sequence since they inherit their ordering from their intended location in memory); and a circuit for generating an

erroneous data verification parameter (ERROR INSERT DECODE circuit 32 in Figure 1 of Khan; Note: ERROR INSERT DECODE circuit 32 can insert erroneous data into D_0, D_1, D_2 and D_3 as well as the parity for D_0, D_1, D_2 and D_3 during special test mode, hence the inserted erroneous data is an erroneous data verification parameter) corresponding to said data unit identified by said data unit identifier (Figure 1 and col. 6, lines 60-68 in Khan teach that D_0 and D_1 are used to identify a data unit of a data unit sequence D_0, D_1, D_2 and D_3 during special test mode) said corresponding erroneous data verification parameter signifying non-verification of data content of said identified data unit (clearly, if erroneous data, i.e., an erroneous data verification parameter, is inserted into the parity coded word, the parity will not be able to establish the accuracy of the word, hence the erroneous data, i.e., an erroneous data verification parameter, signifies non-verification of data content of said identified data unit).

35 U.S.C. 102(b) rejection of claims 2 and 3.

See col. 7, lines 3-15 in Khan.

35 U.S.C. 102(b) rejection of claim 4.

See rejection to claim 1, above.

35 U.S.C. 102(b) rejection of claim 5.

The Examiner would like to point out that since "data content" is written in indefinite form in claims 5 and 11 that the claim language dictates that the "data content" in claims 5

and 11 is referring to an arbitrary data content used to identify "the data content of the identified data unit" as already indicated in claim 1 and that "data content" in claims 5 and 11 is not "the data content of the identified data unit" as already indicated in claim 1. An address is an arbitrary data content (see rejection to claim 1, above).

35 U.S.C. 102(b) rejection of claim 6.

See X-Y ADDRESS DECODE circuit 18 in Figure 1 of Khan. Note; an address is a clear indication of position within a data stream and also position within a memory unit.

35 U.S.C. 102(b) rejection of claim 7.

The limitations in claim 7 are substantially the same as in claim 1 except for the real time testing of a data receiver. The Apparatus of Figure 1 in Khan receives data bits D0-D4, hence is a data receiver. In lines 58-60 of column 15, Khan teaches that the deliberate insertion of an erroneous data bit is carried out in real-time.

35 U.S.C. 102(b) rejection of claims 8 and 9.

See col. 7, lines 3-15 in Khan.

35 U.S.C. 102(b) rejection of claim 10.

See rejection to claim 1, above.

35 U.S.C. 102(b) rejection of claim 11.

The Examiner would like to point out that since "data content" is written in indefinite form in claims 5 and 11 that the claim language dictates that the "data content" in claims 5 and 11 is referring to an arbitrary data content used to identify "the data content of the identified data unit" as already indicated in claim 1 and that "data content" in claims 5 and 11 is not "the data content of the identified data unit" as already indicated in claim 1. An address is an arbitrary data content (see rejection to claim 1, above).

35 U.S.C. 102(b) rejection of claim 12.

See X-Y ADDRESS DECODE circuit 18 in Figure 1 of Khan. Note; an address is a clear indication of position within a data stream and also position within a memory unit.

(11) Response to Argument

[As per claims 1-12]

The Appellant contends, "Khan does not teach identifying a data unit of a data unit sequence wherein the identified data word is not a next data unit of the data unit sequence". The Examiner disagrees and asserts that in Figure 1 of Khan, Khan teaches a device for inserting a parity code into a sequence of data word inputs inputted through terminals D_0, D_1, D_2 and D_3 (Note: the IEEE Authoritative Dictionary of IEEE Standards Terms defines a sequence as a set of items that have been put in a linear arrangement in accordance with the natural numbers, i.e., an ordered set; Note also; that words in memory are an ordered set arranged according to their addresses in memory, hence the input set of words is inherently a sequence since they inherit their

ordering from their intended location in memory). Figure 1 and col. 6, lines 60-68 in Khan teach that inputs to D_0 and D_1 are used to identify a data unit of a data unit sequence inputted to D_0, D_1, D_2 and D_3 during special test modes such as the special test mode for testing of the error check logic. In col. 15, lines 58-60 of Khan, Khan explicitly teaches, "means are provided for enabling the deliberate insertion of an erroneous data bit, to provide a real time electronic simulation of a 'soft' error", hence Khan teaches the deliberate insertion of erroneous bits into an identified data unit belonging to a real-time sequence of data units inputted through terminals D_0, D_1, D_2 and D_3 for real-time testing of the error check logic. In col. 18, lines 25-30, Khan teaches that special test modes are accessed by multiplexing inputs to D_0 and D_1, which can be done since special test modes are performed during read access, hence during special test modes, inputs to D_0, D_1, D_2 and D_3 are not a next data unit of the data unit sequence since they are not written to memory. Figure 1 and col. 6, lines 60-68 in Khan teach that inputs to D_0 and D_1 are used to identify a data unit of a data unit sequence inputted to D_0, D_1, D_2 and D_3 during special test mode wherein the identified data word is not a next data unit of the data unit sequence to be stored in memory since, during special test mode, the identified data unit is not written to memory. Hence, Khan teaches identifying a data unit of a data unit sequence inputted through terminals D_0, D_1, D_2 and D_3 wherein the identified data word is not a next data unit of the data unit sequence that is to be stored in memory, since the identified data unit is for testing only and is not stored in memory as a part of the data unit sequence stored in memory.

[As per claims 7-12]

The Appellant contends, "Khan does not teach real-time testing of a data receiver". The Examiner asserts that the term "real-time" does not have patentable weight. Whether a term in the preamble has patentable weight depends on whether the preamble limits the scope of the claim. In order to make such a determination, the following questions must be answered:

1. Does the preamble language provide antecedent basis for terms in the body of the claim? See Corning Glass works v. Sumitomo Elect. U.S.A., Inc., 9 USPQ2d 1962, 1966 (Fed. Cir. 1989). See In re Paulsen, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

2. Does the language of the body of the claim set out the complete invention? See Allen Eng'g Corp. v. Bartell Indus., Inc., v. Darragh Co., 63 USPQ2d 1769, 1774 (Fed. Cir. 2002).

3. Does the language of the preamble merely provide a statement of purpose or intended use? See DeGeorae v. Bernier, 226 USPQ 758, 761 n.3 (Fed. Cir. 1985).

4. Is the preamble essential to understand limitations or terms in the claim body? See Pitney Bowes, Inc. v. Hewlett-Packard Co., 51 USPQ2d 1161, 1165-66 (Fed. Cir. 1999).

As per question 1, the term "real-time" does not provide antecedent basis for terms in the body of the claim, therefore, has no patentable weight based on antecedent basis. As per question 2, the language of the body of the claim sets out the complete invention since the term "real-time" is only a descriptive term for the limitation, "a data unit identifier for identifying a data unit other than a next data unit to be transferred in a data unit sequence", that is; "identifying a data unit other than a next data unit to be

transferred in a data unit sequence" is a real-time operation, therefore, the body of the claim is inherently a method for real-time testing, hence the term "real-time" has no patentable weight based on analysis of the second question (Note: in lines 15-19 on page 7 of the Appellant's Appeal Brief, the Appellant admits that the limitation "identifying a data unit other than a next data unit to be transferred in a data unit sequence" is an operation for real-time testing).

As per question 3, the term "real-time" merely provides a statement of purpose and intended use (Note: in the Appellant's own admission in lines 15-19 on page 7 of the Appellant's Appeal Brief, the Appellant admits that the limitation "identifying a data unit other than a next data unit to be transferred in a data unit sequence" is an operation for real-time testing, hence the term "real-time" merely provides an indication of purpose and intent).

As per question 4, since the term "real-time" merely provides a statement of purpose and intended use, it is not essential to the understanding of limitations within the body of the claim.

Based on the analysis above, the term does not have patentable weight.

Arguendo, even if the preamble were to be considered, Khan in col. 15, lines 58-60 explicitly teaches, "means are provided for enabling the deliberate insertion of an erroneous data bit, to provide a real time electronic simulation of a 'soft' error" in reference to the error insertion means taught in the Kahn patent (see col. 15, lines 46-60, Khan). Hence, the special testing function for inserting erroneous data to verify

operation of the check word generating circuitry at the receiving side of the memory array is a real-time test for a data receiver (Note: Sense Amplifier 14 and Bit Error Correction Means 22 in Figure 1 of Khan are part of the receiving unit used for receiving data from memory and correcting the data).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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